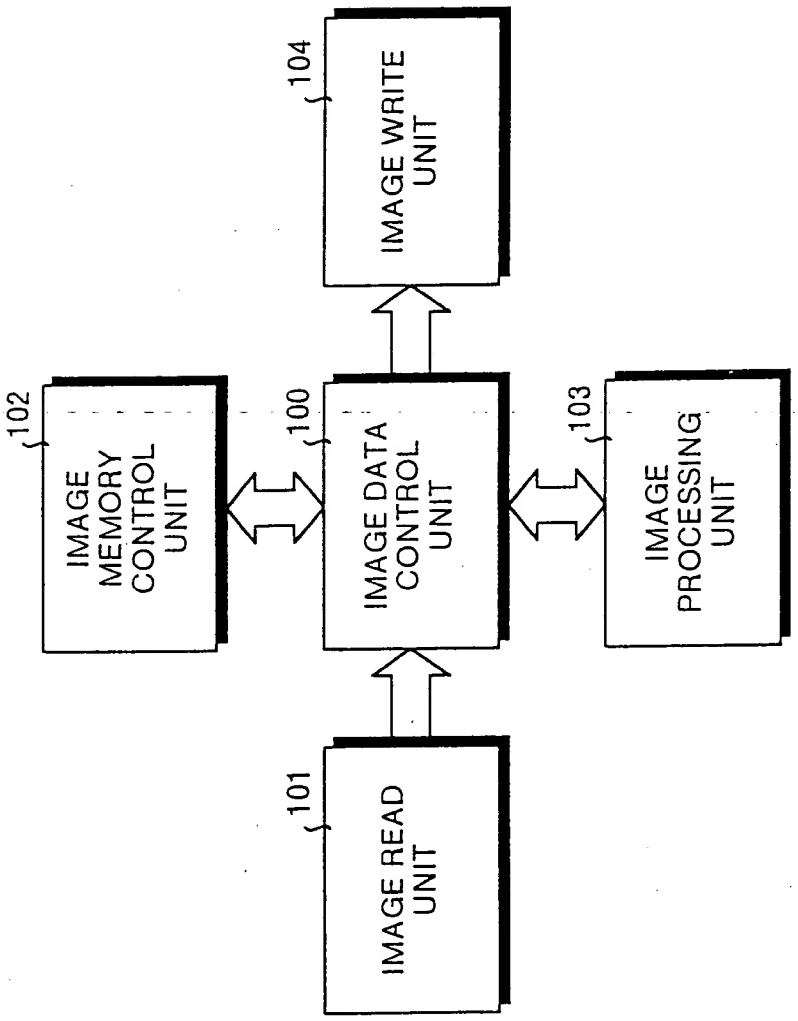
FIG.1


104
IMAGE WRITE UNIT
102
IMAGE MEMORY CONTROL UNIT
100
IMAGE DATA CONTROL UNIT
103
IMAGE PROCESSING UNIT
101
IMAGE READ UNIT

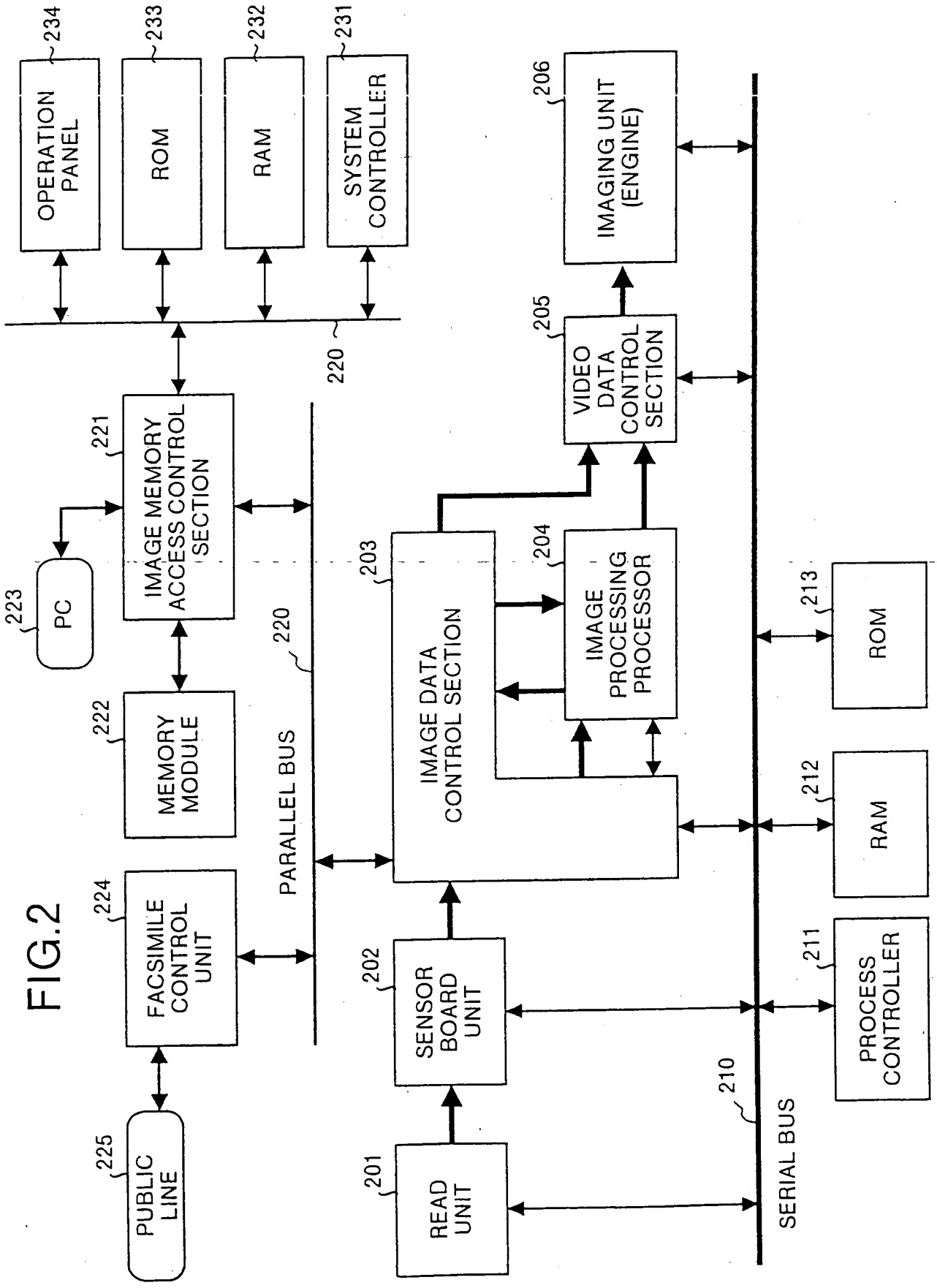

OPERATION PANEL
234
ROM
233
RAM
232
SYSTEM CONTROLLER
231
220
IMAGING UNIT (ENGINE)
206
VIDEO DATA CONTROL SECTION
205
IMAGE MEMORY ACCESS CONTROL SECTION
221
PC
223
MEMORY MODULE
222
PARALLEL BUS
220
IMAGE DATA CONTROL SECTION
203
IMAGE PROCESSING PROCESSOR
204
ROM
213
RAM
212
FACSIMILE CONTROL UNIT
224
SENSOR BOARD UNIT
202
PROCESS CONTROLLER
211
PUBLIC LINE
225
READ UNIT
201
SERIAL BUS
210

FIG.2

FIG.3

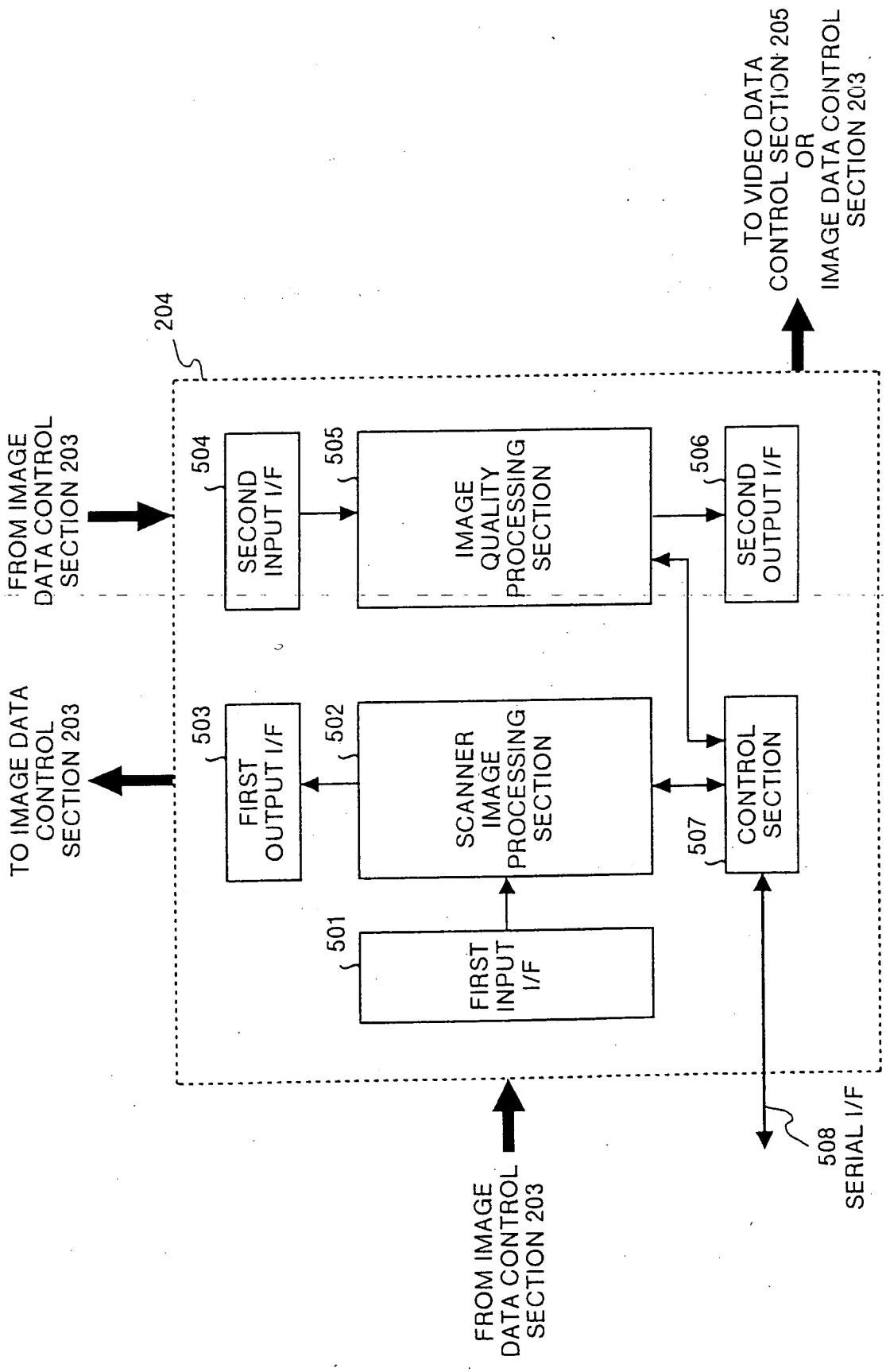

204
FROM IMAGE DATA CONTROL SECTION 203
TO VIDEO DATA CONTROL SECTION 205 OR IMAGE DATA CONTROL SECTION 203
504
SECOND INPUT I/F
505
IMAGE QUALITY PROCESSING SECTION
506
SECOND OUTPUT I/F
TO IMAGE DATA CONTROL SECTION 203
503
FIRST OUTPUT I/F
502
SCANNER IMAGE PROCESSING SECTION
507
CONTROL SECTION
501
FIRST INPUT I/F
FROM IMAGE DATA CONTROL SECTION 203
508
SERIAL I/F

FIG.4

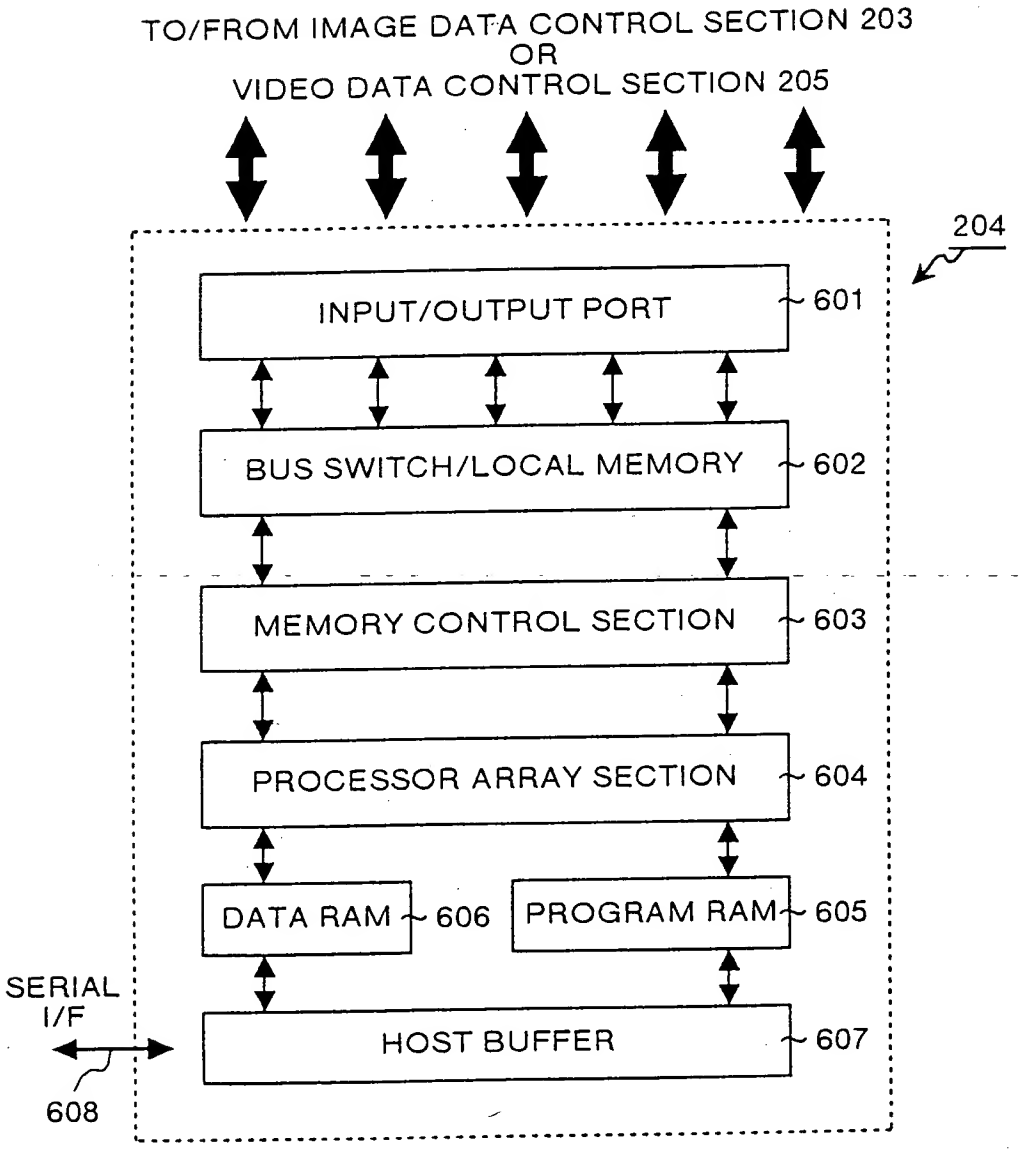

TO/FROM IMAGE DATA CONTROL SECTION 203
OR
VIDEO DATA CONTROL SECTION 205
204
INPUT/OUTPUT PORT
601
BUS SWITCH/LOCAL MEMORY
602
MEMORY CONTROL SECTION
603
PROCESSOR ARRAY SECTION
604
DATA RAM
606
PROGRAM RAM
605
HOST BUFFER
607
SERIAL
I/F
608

FIG.5

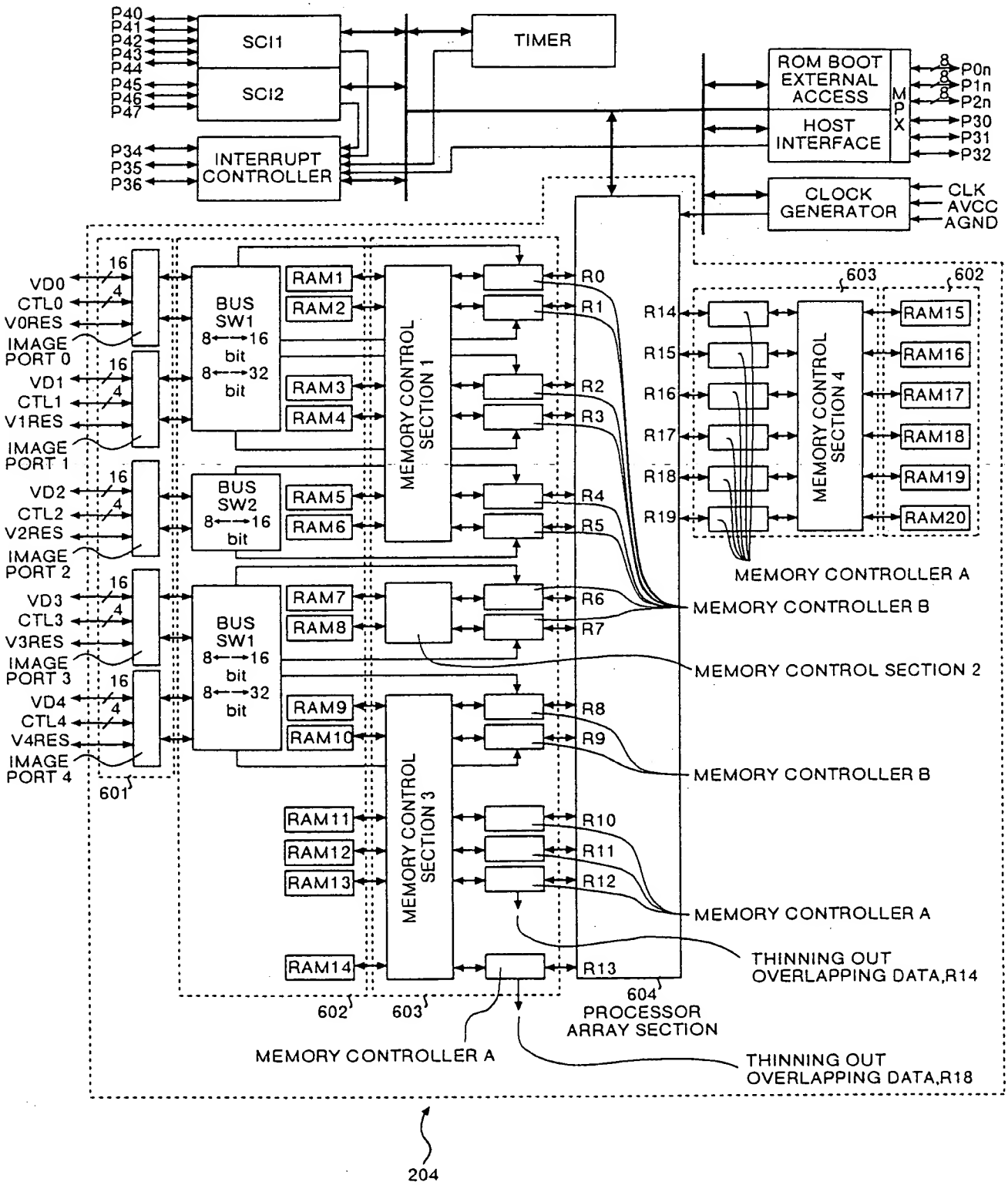

P40
P41
P42
P43
P44
P45
P46
P47
P34
P35
P36
SCI1
SCI2
INTERRUPT CONTROLLER
TIMER
ROM BOOT EXTERNAL ACCESS
HOST INTERFACE
MPX
8 P0n
8 P1n
8 P2n
P30
P31
P32
CLOCK GENERATOR
CLK
AVCC
AGND
VD0
CTL0
V0RES
IMAGE PORT 0
VD1
CTL1
V1RES
IMAGE PORT 1
VD2
CTL2
V2RES
IMAGE PORT 2
VD3
CTL3
V3RES
IMAGE PORT 3
VD4
CTL4
V4RES
IMAGE PORT 4
16
4
601
BUS SW1 8←→16 bit 8←→32 bit
BUS SW2 8←→16 bit
RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7
RAM8
RAM9
RAM10
RAM11
RAM12
RAM13
RAM14
MEMORY CONTROL SECTION 1
MEMORY CONTROL SECTION 3
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
603
602
RAM15
RAM16
RAM17
RAM18
RAM19
RAM20
MEMORY CONTROL SECTION 4
MEMORY CONTROLLER A
MEMORY CONTROLLER B
MEMORY CONTROL SECTION 2
MEMORY CONTROLLER B
MEMORY CONTROLLER A
THINNING OUT OVERLAPPING DATA,R14
THINNING OUT OVERLAPPING DATA,R18
604
PROCESSOR ARRAY SECTION
602
603
MEMORY CONTROLLER A
204

FIG.6

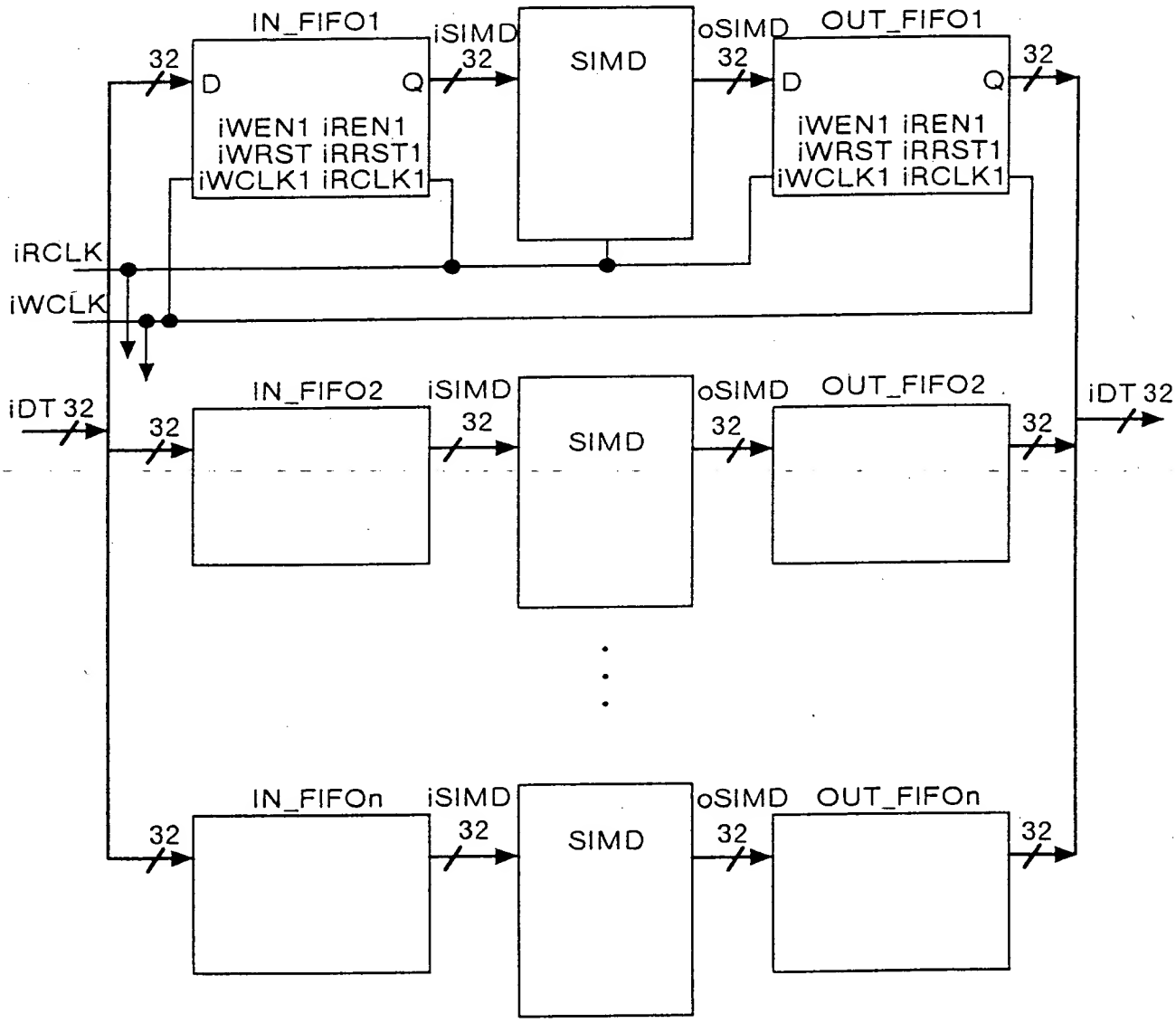

IN_FIFO1
iSIMD
32
SIMD
oSIMD
32
OUT_FIFO1
32
D
Q
iWEN1 iREN1
iWRST iRRST1
iWCLK1 iRCLK1
iRCLK
iWCLK
iDT 32
IN_FIFO2
OUT_FIFO2
IN_FIFOn
OUT_FIFOn

FIG.7

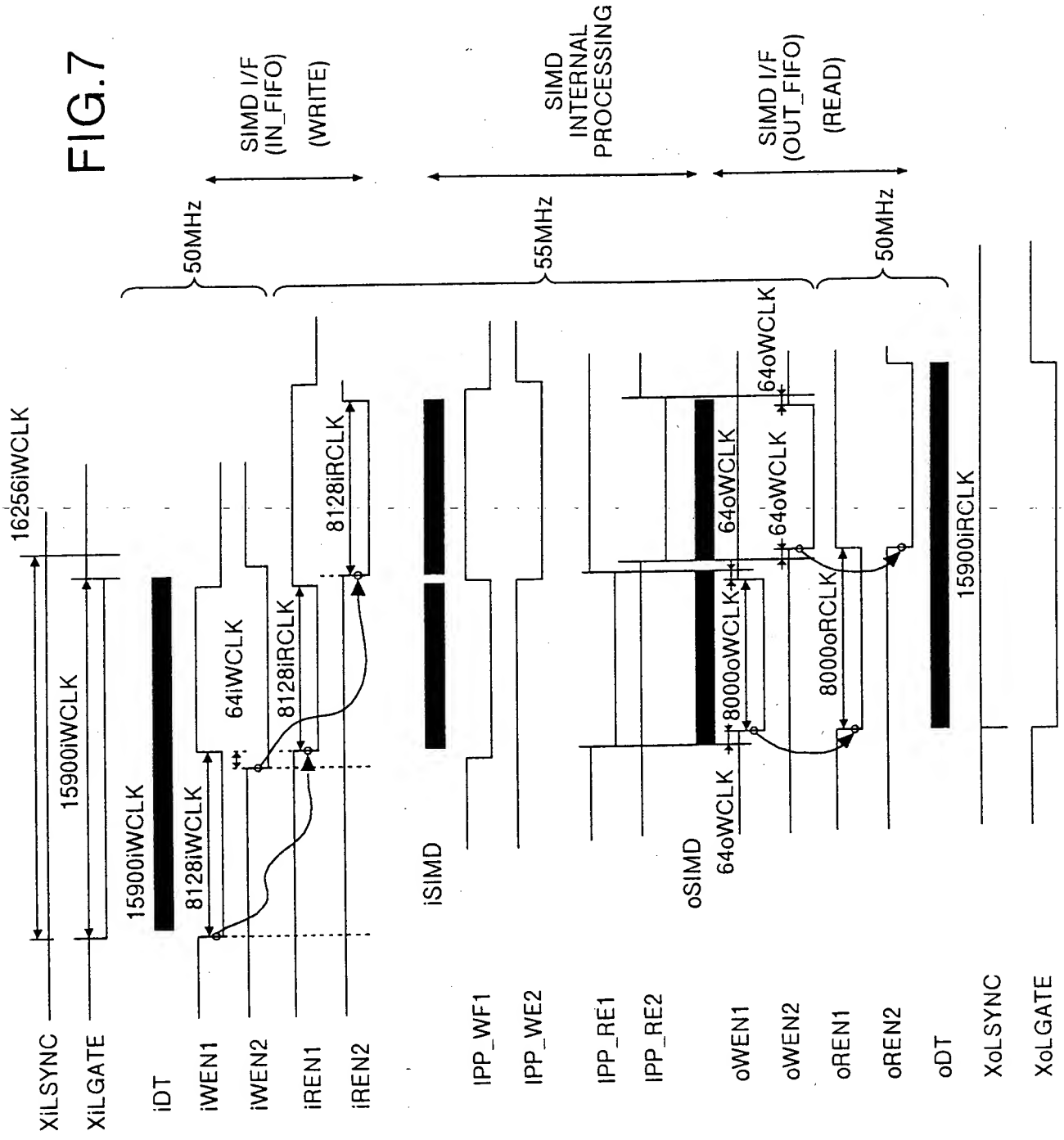
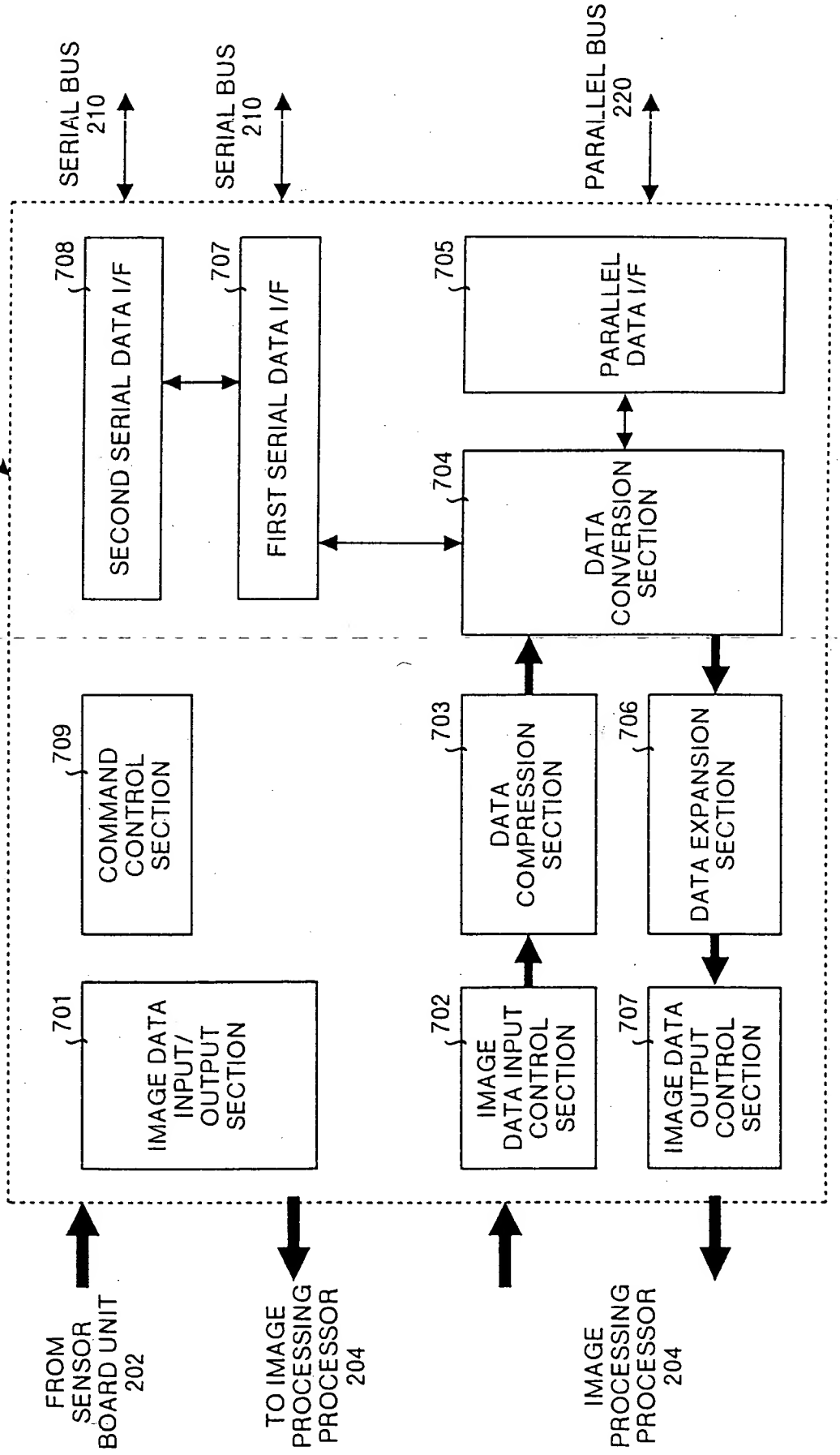

SIMD I/F (IN_FIFO) (WRITE)
SIMD INTERNAL PROCESSING
SIMD I/F (OUT_FIFO) (READ)
50MHz
55MHz
50MHz
16256iWCLK
15900iWCLK
15900iWCLK
8128iWCLK
64iWCLK
8128iRCLK
8128iRCLK
640oWCLK
640oWCLK
640oWCLK
8000oWCLK
8000oRCLK
15900iRCLK
XiLSYNC
XiLGATE
iDT
iWEN1
iWEN2
iREN1
iREN2
iSIMD
IPP_WF1
IPP_WE2
IPP_RE1
IPP_RE2
oSIMD
oWEN1
oWEN2
oREN1
oREN2
oDT
XoLSYNC
XoLGATE

FIG.8


SERIAL BUS 210
SERIAL BUS 210
PARALLEL BUS 220
203
708
SECOND SERIAL DATA I/F
707
FIRST SERIAL DATA I/F
705
PARALLEL DATA I/F
704
DATA CONVERSION SECTION
709
COMMAND CONTROL SECTION
703
DATA COMPRESSION SECTION
706
DATA EXPANSION SECTION
701
IMAGE DATA INPUT/ OUTPUT SECTION
702
IMAGE DATA INPUT CONTROL SECTION
707
IMAGE DATA OUTPUT CONTROL SECTION
FROM SENSOR BOARD UNIT 202
TO IMAGE PROCESSING PROCESSOR 204
IMAGE PROCESSING PROCESSOR 204

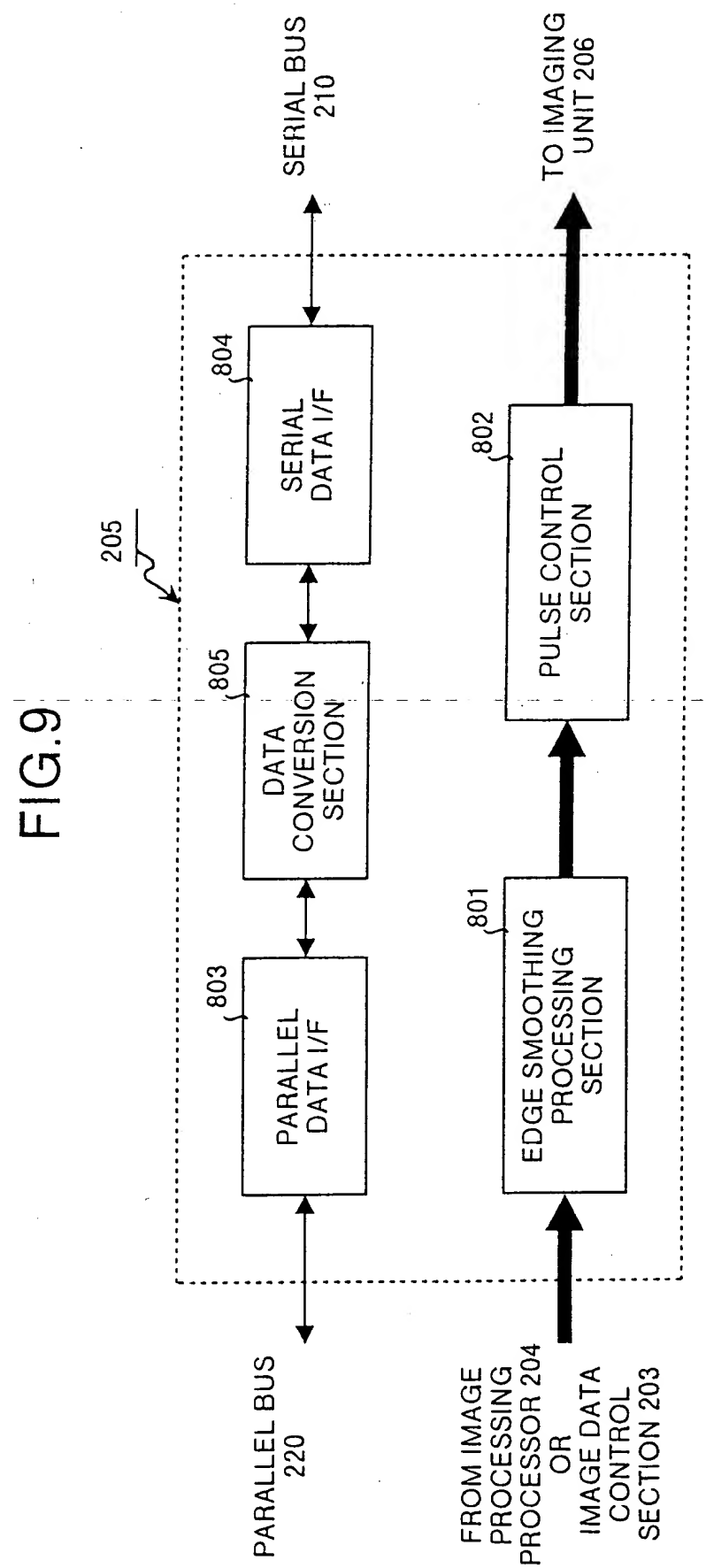

205
SERIAL BUS 210
TO IMAGING UNIT 206
804
SERIAL DATA I/F
802
PULSE CONTROL SECTION
805
DATA CONVERSION SECTION
801
EDGE SMOOTHING PROCESSING SECTION
803
PARALLEL DATA I/F
PARALLEL BUS 220
FROM IMAGE PROCESSING PROCESSOR 204 OR IMAGE DATA CONTROL SECTION 203

FIG.9

FIG.10

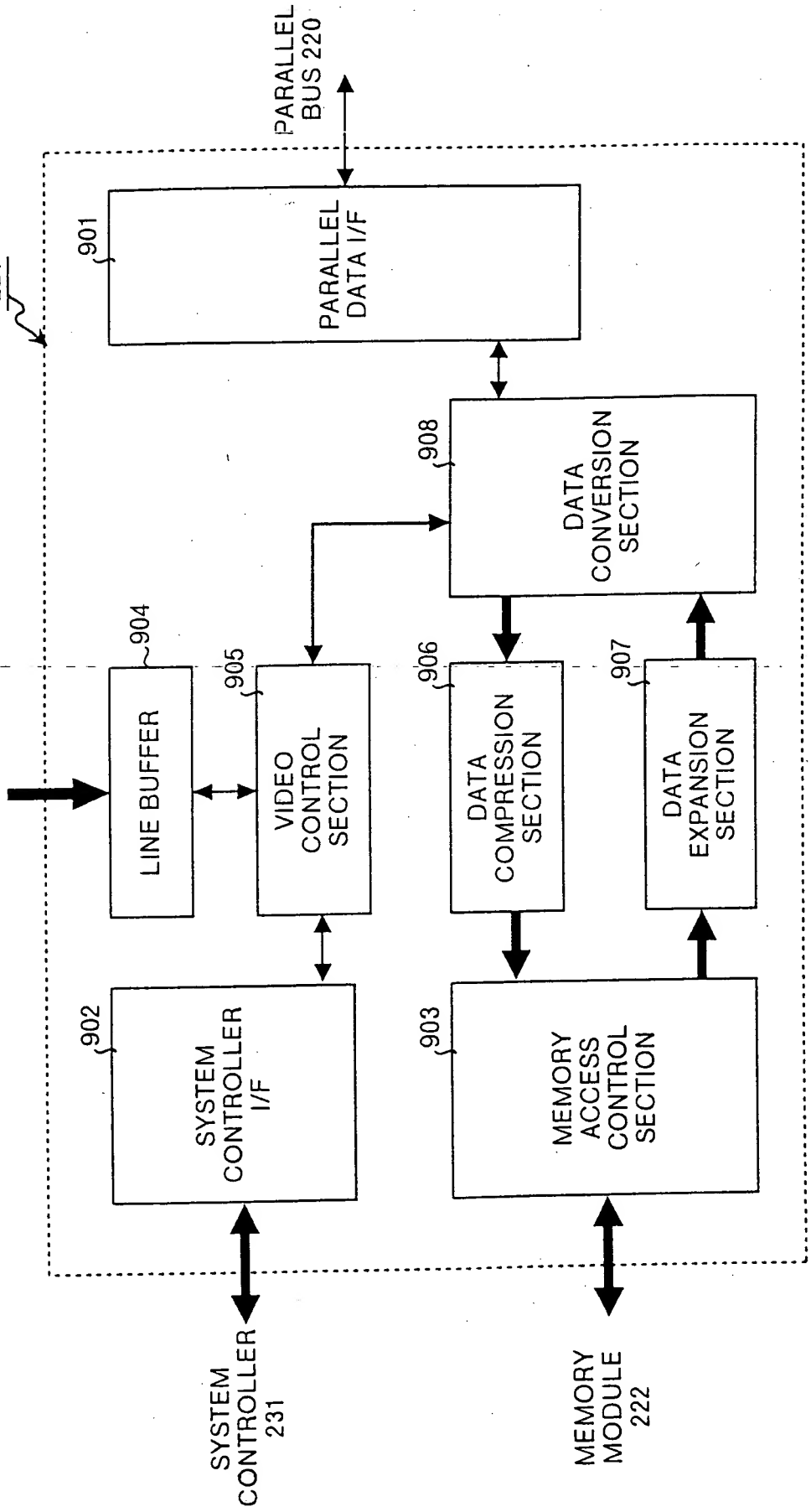

PARALLEL BUS 220
221
901
PARALLEL DATA I/F
908
DATA CONVERSION SECTION
904
905
906
907
FROM PC 223
LINE BUFFER
VIDEO CONTROL SECTION
DATA COMPRESSION SECTION
DATA EXPANSION SECTION
902
903
SYSTEM CONTROLLER I/F
MEMORY ACCESS CONTROL SECTION
SYSTEM CONTROLLER 231
MEMORY MODULE 222

FIG.11

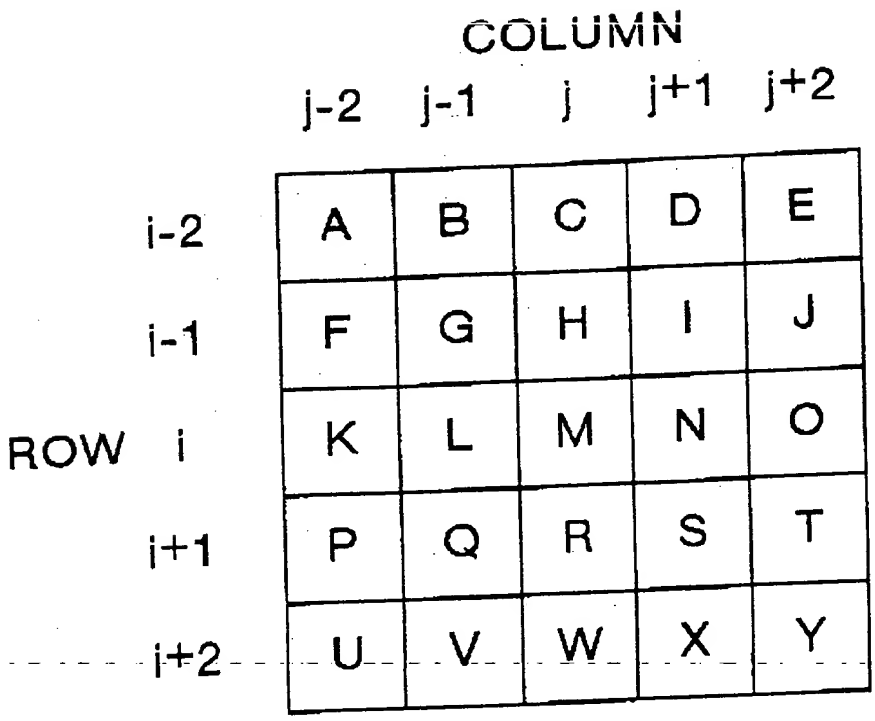
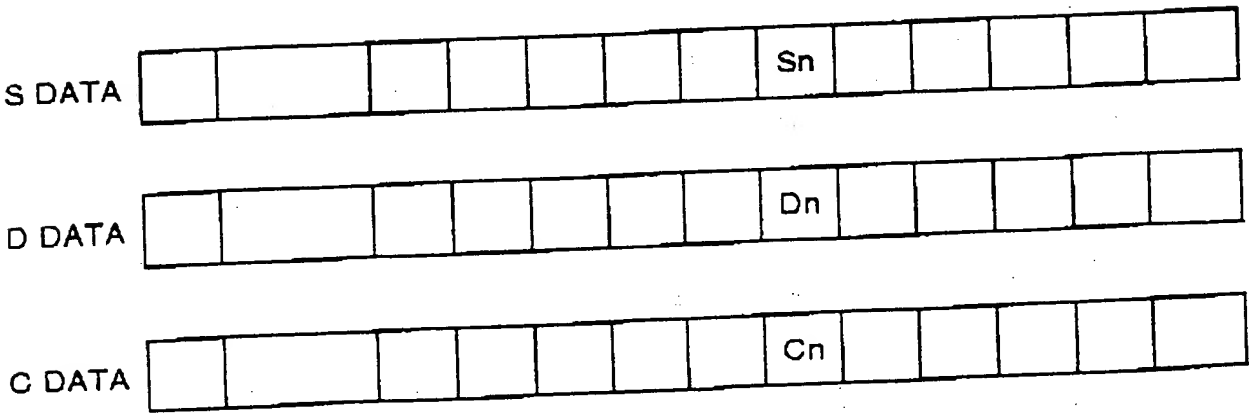

COLUMN
j-2
j-1
j
j+1
j+2
ROW i
i-2
i-1
i+1
i+2
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y

FIG.12


S DATA
Sn
D DATA
Dn
C DATA
Cn

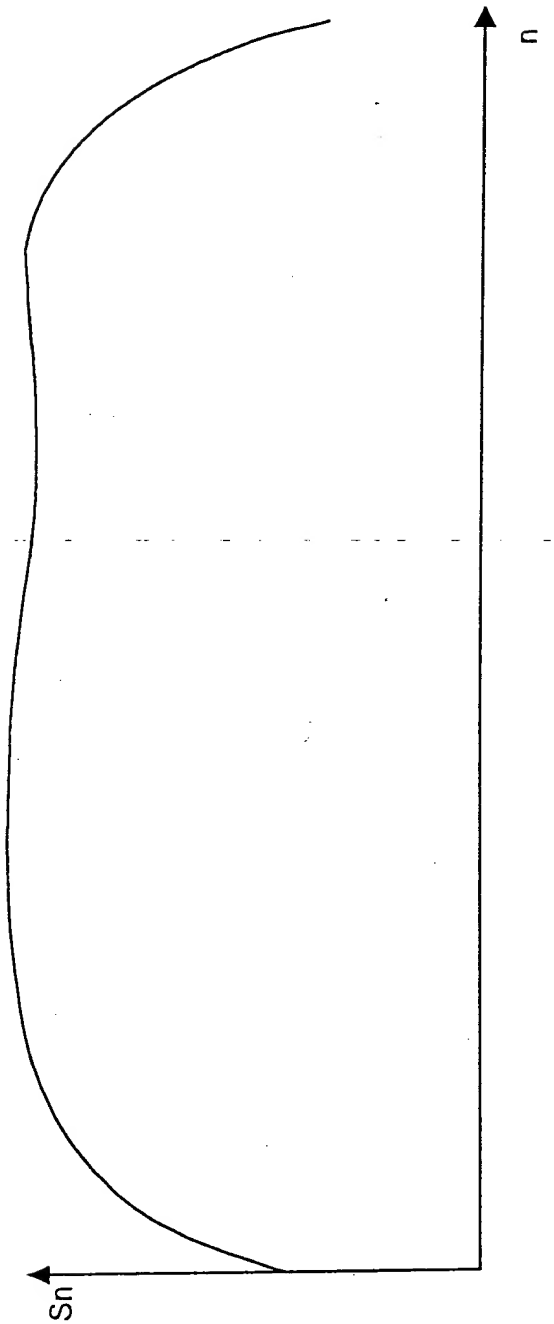


FIG.13

FIG.14

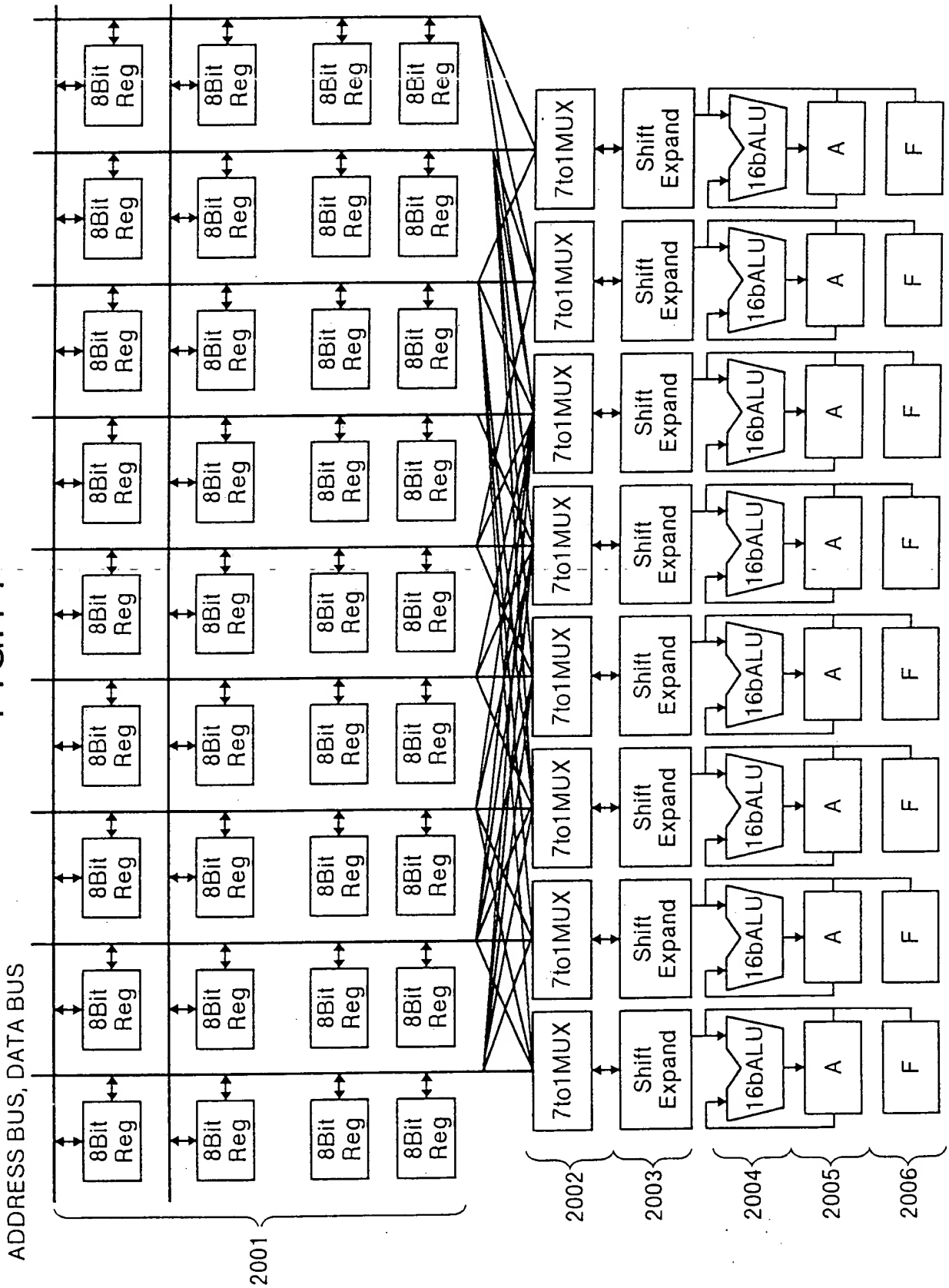

ADDRESS BUS, DATA BUS
8Bit Reg
7to1MUX
Shift Expand
16bALU
A
F
2001
2002
2003
2004
2005
2006

FIG.15

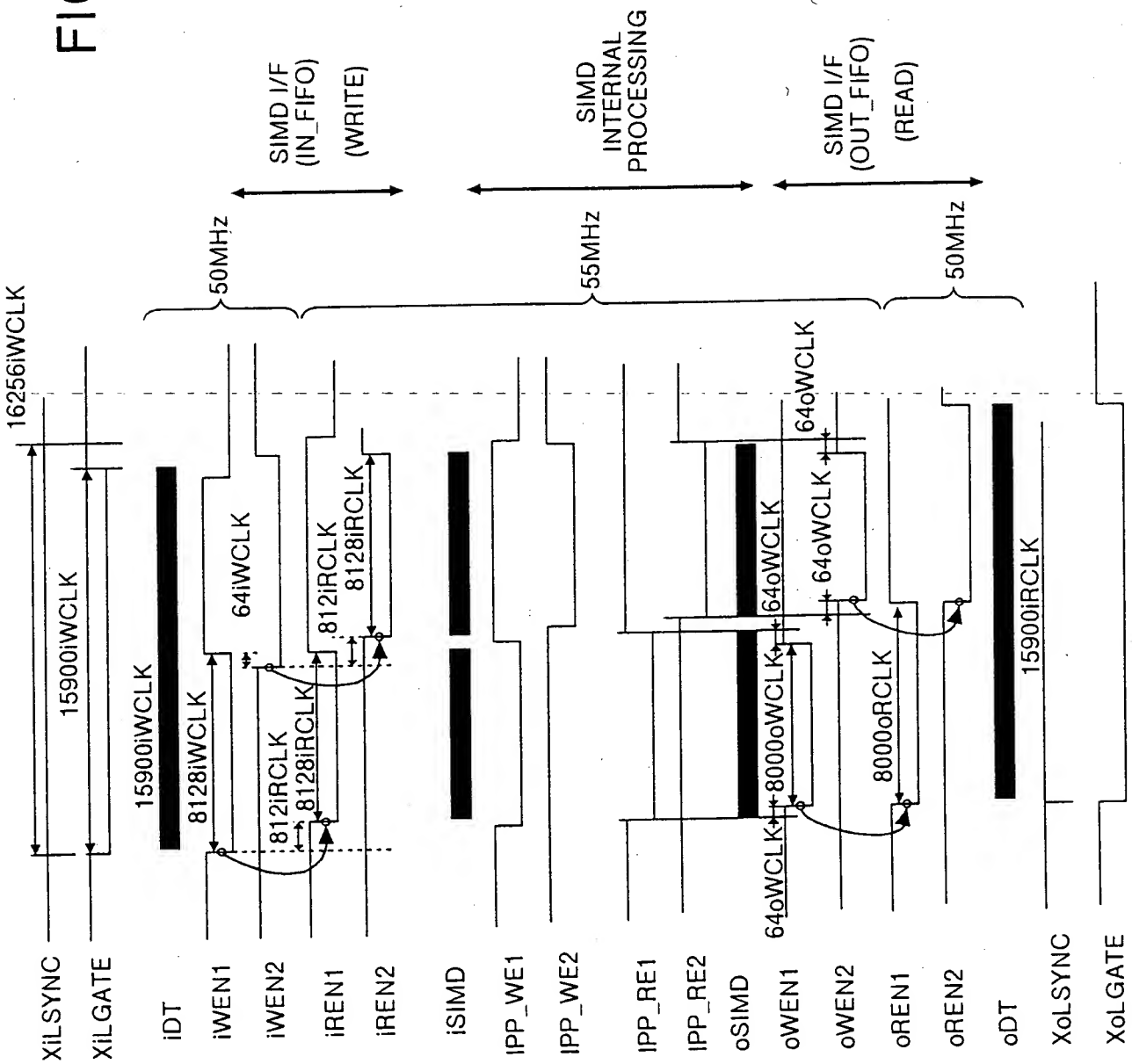

SIMD I/F (IN_FIFO) (WRITE)
SIMD INTERNAL PROCESSING
SIMD I/F (OUT_FIFO) (READ)
50MHz
55MHz
50MHz
16256iWCLK
15900iWCLK
8128iWCLK
64iWCLK
812iRCLK
8128iRCLK
640WCLK
8000oWCLK
8000oRCLK
15900iRCLK
XiLSYNC
XiLGATE
iDT
iWEN1
iWEN2
iREN1
iREN2
iSIMD
IPP_WE1
IPP_WE2
IPP_RE1
IPP_RE2
oSIMD
oWEN1
oWEN2
oREN1
oREN2
oDT
XoLSYNC
XoLGATE

FIG.16

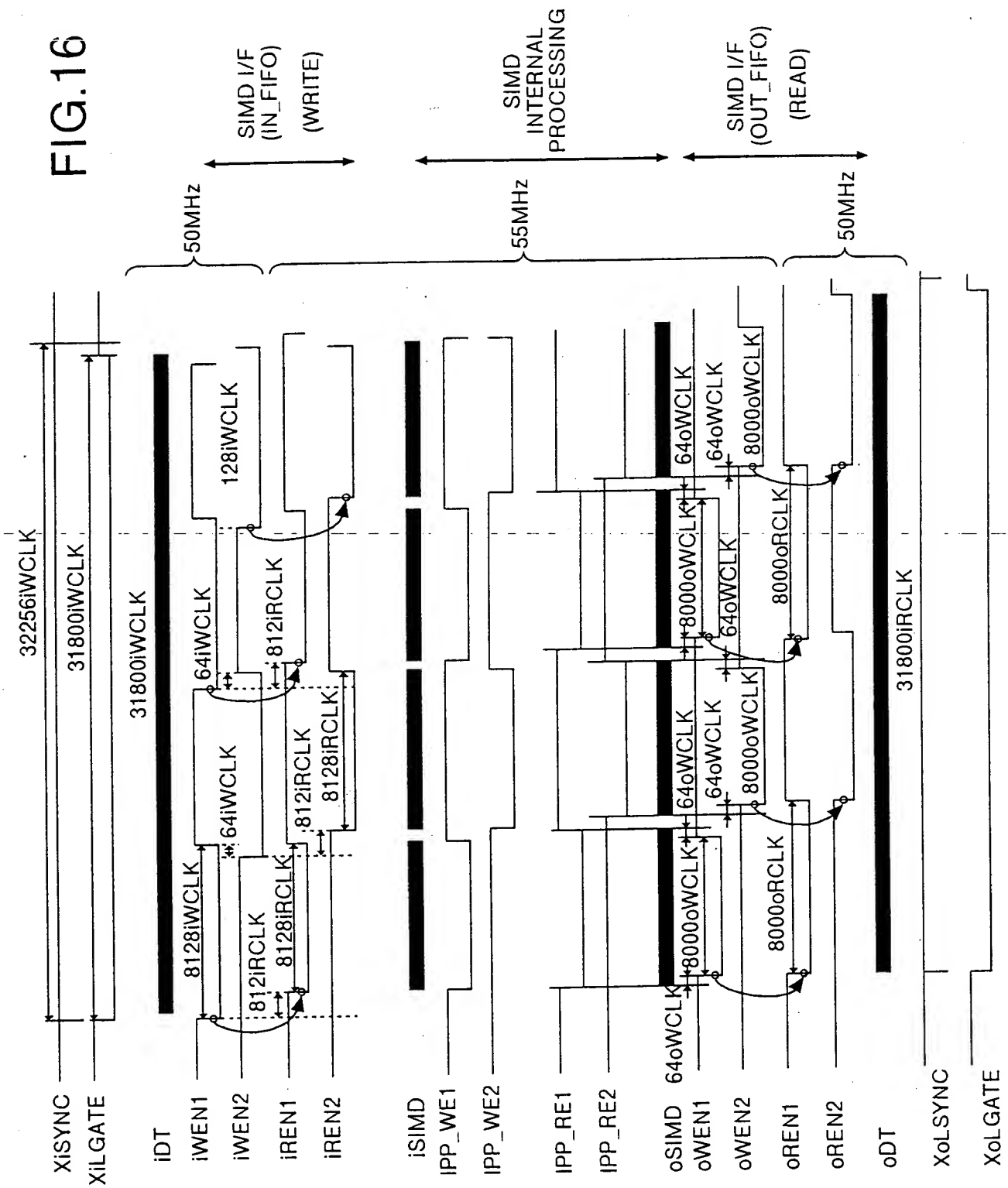

SIMD I/F (IN_FIFO) (WRITE)
SIMD INTERNAL PROCESSING
SIMD I/F (OUT_FIFO) (READ)
50MHz
55MHz
50MHz
32256iWCLK
31800iWCLK
31800iWCLK
128iWCLK
64iWCLK
812iRCLK
8128iWCLK
64iWCLK
812iRCLK
8128iRCLK
812iRCLK
8128iRCLK
31800iRCLK
64oWCLK
8000oWCLK
8000oRCLK
XiSYNC
XiLGATE
iDT
iWEN1
iWEN2
iREN1
iREN2
iSIMD
IPP_WE1
IPP_WE2
IPP_RE1
IPP_RE2
oSIMD
oWEN1
oWEN2
oREN1
oREN2
oDT
XoLSYNC
XoLGATE

FIG.17

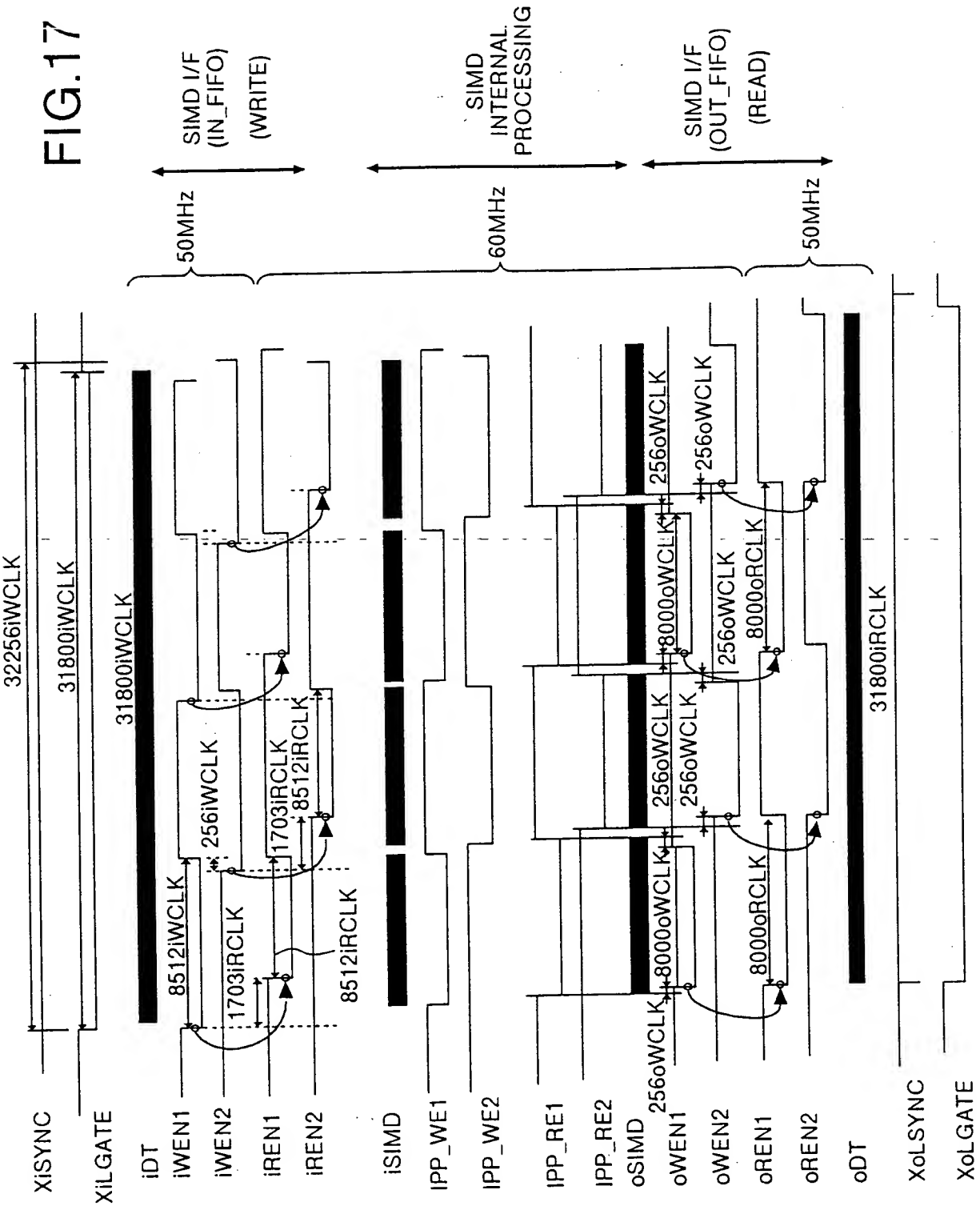
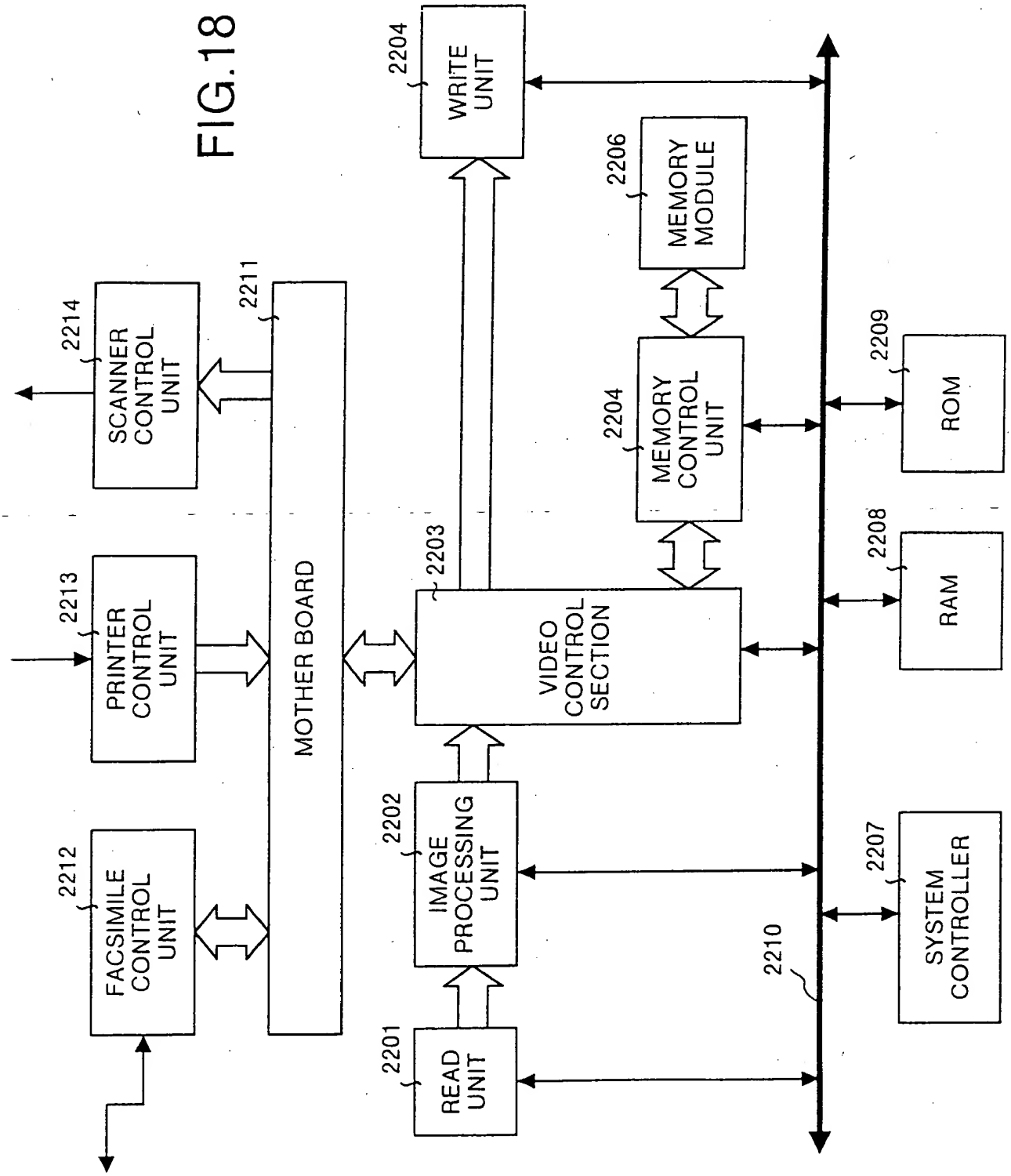

SIMD I/F (IN_FIFO) (WRITE)
SIMD INTERNAL PROCESSING
SIMD I/F (OUT_FIFO) (READ)
50MHz
60MHz
50MHz
32256iWCLK
31800iWCLK
31800iWCLK
8512iWCLK
256iWCLK
1703iRCLK
1703iRCLK
8512iRCLK
8512iRCLK
256oWCLK
8000oWCLK
256oWCLK
256oWCLK
8000oWCLK
256oWCLK
256oWCLK
8000oRCLK
8000oRCLK
31800iRCLK
XiSYNC
XiLGATE
iDT
iWEN1
iWEN2
iREN1
iREN2
iSIMD
IPP_WE1
IPP_WE2
IPP_RE1
IPP_RE2
oSIMD
oWEN1
oWEN2
oREN1
oREN2
oDT
XoLSYNC
XoLGATE

FIG.18


2204
WRITE UNIT
2206
MEMORY MODULE
2214
SCANNER CONTROL UNIT
2211
2204
MEMORY CONTROL UNIT
2209
ROM
2213
PRINTER CONTROL UNIT
MOTHER BOARD
2203
VIDEO CONTROL SECTION
2208
RAM
2212
FACSIMILE CONTROL UNIT
2202
IMAGE PROCESSING UNIT
2207
SYSTEM CONTROLLER
2210
2201
READ UNIT